

REMARKS

Claims 1-6 are rejected under 35 U.S.C. § 102(e) as being anticipated by Inaba, *et al.* (U.S. Patent Number 6,650,590). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

The applicant notes that the Office Action refers to the Sugawara reference at line 5 on page 3. The applicant assumes that the Examiner intended to refer to the Inaba, *et al.* reference.

The applicant's invention is directed to a word line driver circuit of a semiconductor memory device in which main word line signals are generated to enable a plurality of main word lines. A voltage supply unit of the invention supplies a first voltage to a first node during a first time interval and then supplies a second voltage, that is higher than the first voltage, to the first node for a second time interval that occurs later than the first time interval. That is, the second voltage is applied to the first node after the first voltage is applied. A plurality of output units that generate a respective plurality of word line signals are connected to the first node. Each output unit receives a precharge signal PRECH and a decoded row address signal, e.g., DRA1, and, in response to those input signals, generates a respective word line signal. Each output unit includes a second node which is connected through a transistor to the first node when the transistor is activated via the decoded row address signal, e.g., DRA1, such that the first and second voltages are received at the second node within the output unit. The voltage at the second node is inverted to produce the respective main word line signal output by the output unit.

These specific features of the invention are now set forth in the amended claims. That is, the claims are amended to clarify these specific details of the invention. It is believed that, with these clarifying amendments, the claims now clearly distinguish the Inaba, *et al.* reference.

Inaba, *et al.* teach level shifting circuits in a local word drive line driving circuit applied to a semiconductor memory device. Inaba, *et al.* is cited as teaching the applicant's claimed main word line driver circuit of a semiconductor memory device, including a voltage supply unit supplying first and second voltages to a node and a plurality of output units receiving the first voltage supply to the node and generating respective main word line signals.

However, Inaba, *et al.* fail to teach or suggest the specific features now set forth in the

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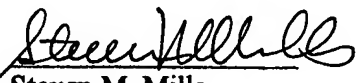
amended claims. Specifically, Inaba, *et al.* neither teach nor suggest a first voltage and a second voltage being applied to a single node at first and second time intervals, respectively, wherein the second time interval is after the first time interval. Furthermore, Inaba, *et al.* fail to teach or suggest output units receiving a precharge signal and a decoded row address signal and having a second node that is inverted by an inverter to generate the main word line signal output by the output unit. The Inaba, *et al.* reference also fails to teach or suggest the second node of the output units being connected to the first node through a transistor which is activated by a decoded row address signal such that the second node in the output unit receives the first and second voltages generated by the voltage supply unit in response to the decoded row address signal.

Accordingly, Inaba, *et al.* fail to teach or suggest the invention set forth in the amended claims. Therefore, it is believed that the amended claims are allowable over Inaba, *et al.*, and, therefore, reconsideration of the rejections of claims 1-6 under 35 U.S.C. § 102(e) as being anticipated by Inaba, *et al.* is respectfully requested.

In view of the amendments to the specification and the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: March 22, 2005
Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
C:\Documents and Settings\smills\Desktop\amendmenta.wpd


Steven M. Mills
Registration Number 36,610
Attorney for Applicants